Island-Style Monolithic Three-Dimensional CMOS-Nanoelectromechanical Logic Circuits

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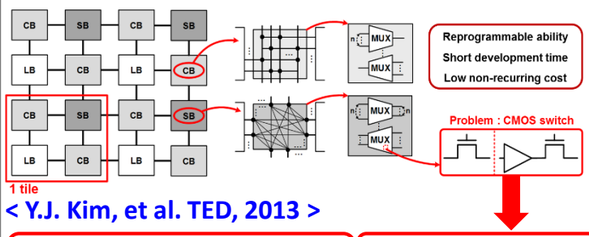
Motivation

Limits of CMOS-only FPGAs



< Y.J. Kim, et al. TED, 2013 >

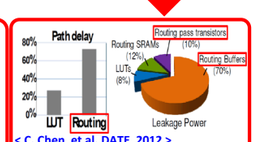
Reprogrammable ability
Short development time
Low non-recurring cost

Problem : CMOS switch

CMOS routing block

- High power consumption
- Large circuit delay
- Large chip area

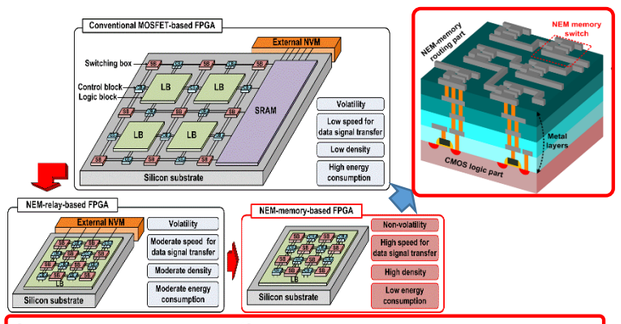
CMOS routing block (SB/CB) should be changed for low-power/large-density FPGA!



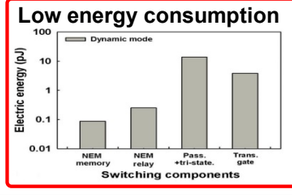
< C. Chen, et al. DATE, 2012 >
< C. Chen, et al. ACM/SIGMA FPGA, 2012 >

Over 70% of delay and leakage originates from CMOS routers.

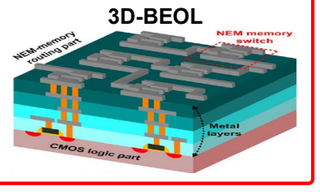
Merits of CMOS-NEM FPGAs



Low energy consumption



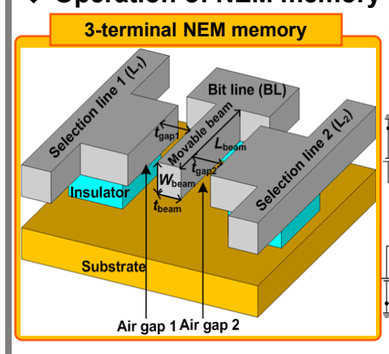
3D-BEOL



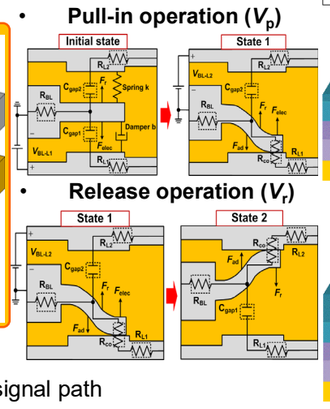
Ideas

Basic structure of NEM switches

◆ Operation of NEM memory switches

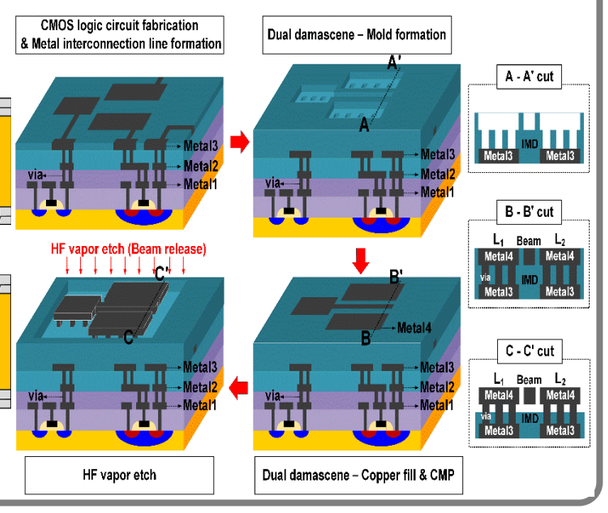


- Pull-in operation (V_p)
- Release operation (V_r)



- Zero voltage → beam stiction
  - ⇒ Nonvolatile & stable data signal path
  - ⇒ Switching voltage (V_s) is determined by max(V_p, V_r)

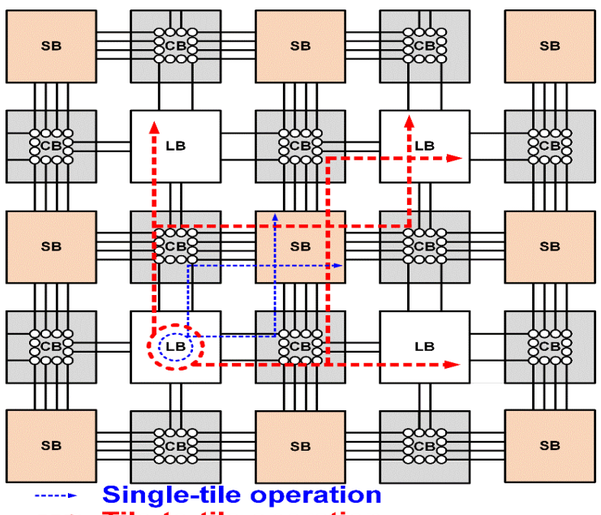
M3D integration process



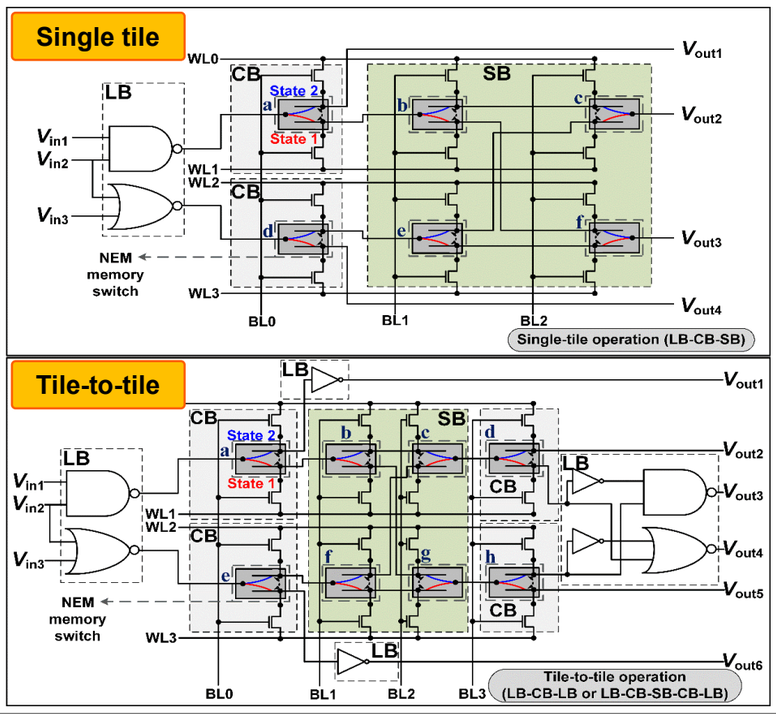
Method

Island style M3D CMOS-NEM RL circuits

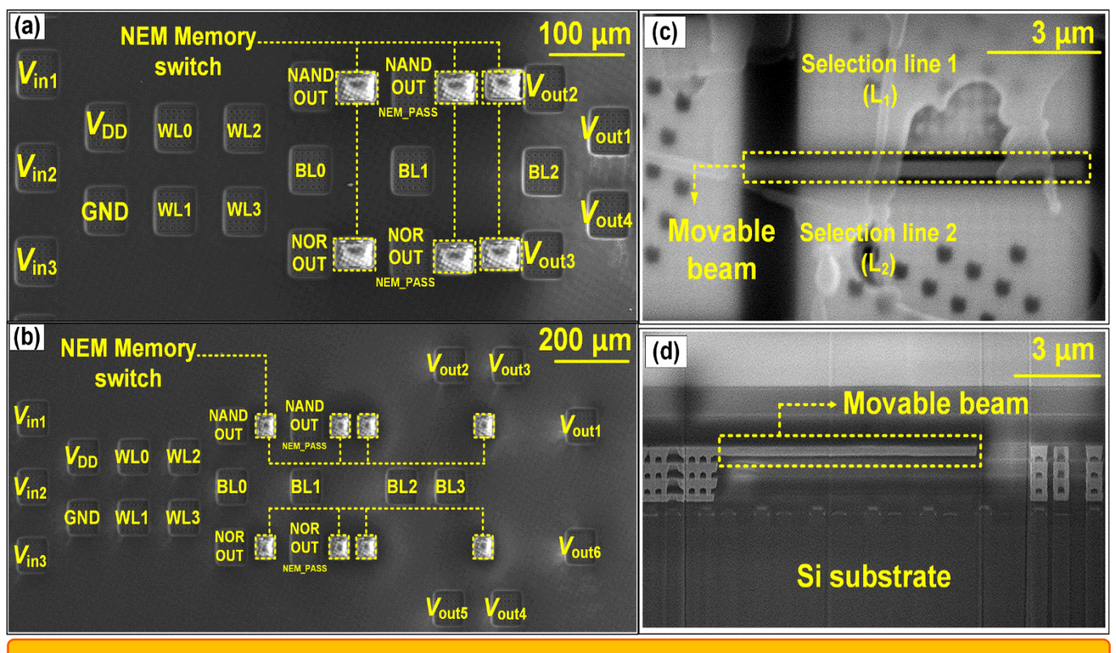
➢Consists of single tile and tile-to-tile CMOS-NEM RL circuits



Schematic view of the island-style RL structure representing single-tile and tile-to-tile operation



Fabricated M3D CMOS-NEM RL circuit



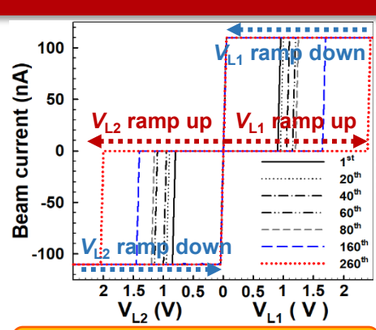
Plan view of the fabricated M3D CMOS-NEM RL circuit for (a) single-tile operation and (b) tile-to-tile operation. (c) Plan and (d) cross-sectional view of the fabricated NEM memory switch

Experimental Result

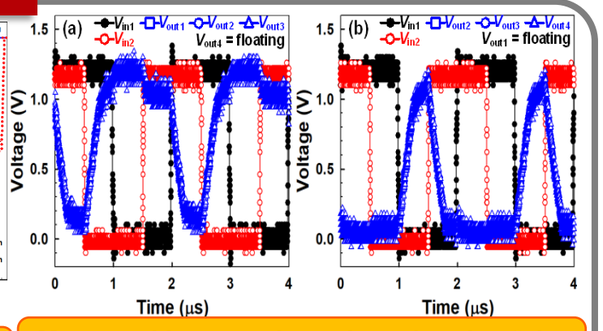
➢NEM memory switch operates **under 1.2 V till ~ 80th cycle** (maximum cycle : 260th)

➢No difference between V_{out1} and V_{beam}
- ✓ Due to low resistive copper lines (1.68 μΩ·cm)

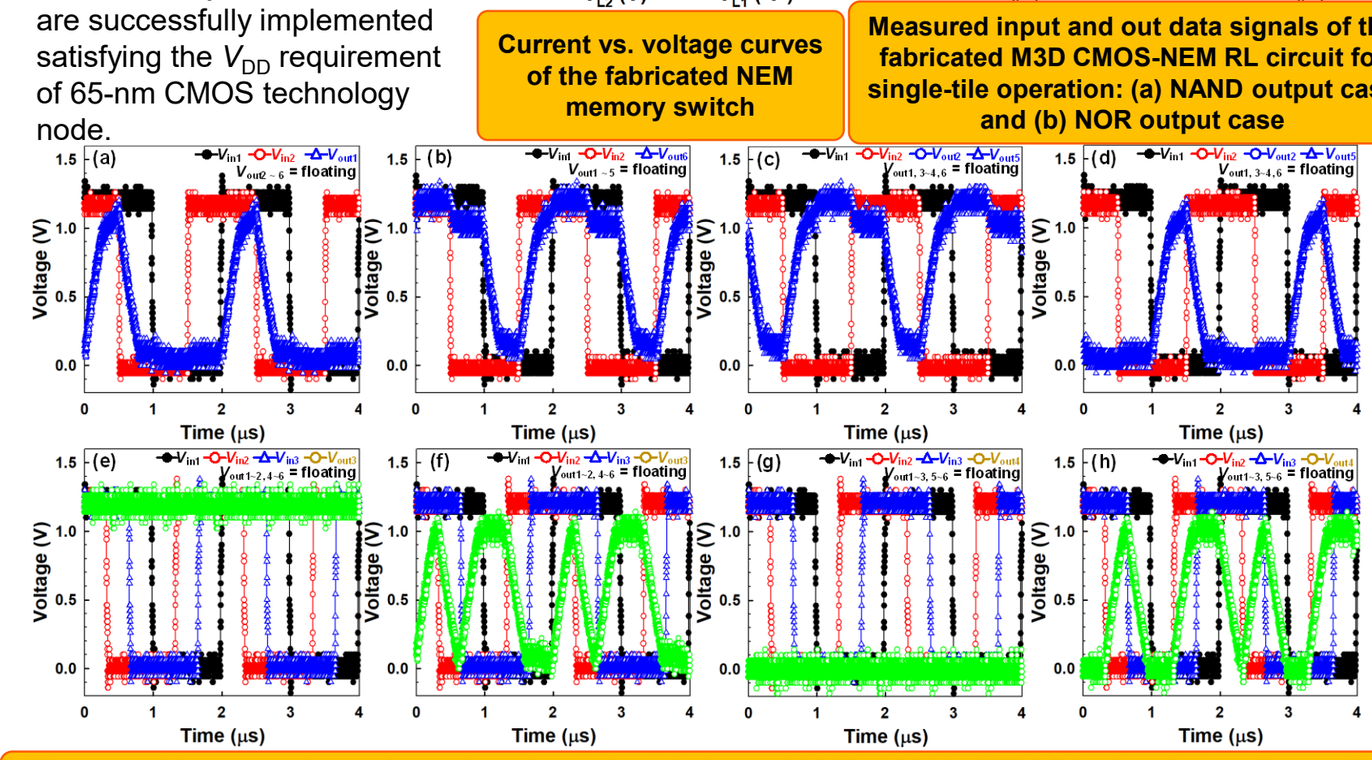
➢NEM memory based RL circuits are successfully implemented satisfying the V_{DD} requirement of 65-nm CMOS technology node.



Current vs. voltage curves of the fabricated NEM memory switch



Measured input and out data signals of the fabricated M3D CMOS-NEM RL circuit for single-tile operation: (a) NAND output case and (b) NOR output case



Measured input and out data signals of the fabricated M3D CMOS-NEM RL circuit for tile-to-tile operation: (a) V_{in1}*V_{in2} output case, (b) V_{in2}+V_{in3} output case, (c) NAND output case, (d) NOR output case, (e) /((V_{in1}*V_{in2}) * /(V_{in2}+V_{in3})) output case, (f) /((V_{in2}+V_{in3}) * /(V_{in1}*V_{in2})) output case, (g) /(/(V_{in1}*V_{in2}) + (V_{in2}+V_{in3})) output case and (h) /(/(V_{in2}+V_{in3}) + (V_{in1}*V_{in2})) output case.

Analysis

Comparison of RL circuit operation

Simulation was carried out by replacing CB & SB parts of the circuit.

Operation	Single-tile operation				Tile to tile operation			
RL circuit	M3D CMOS-NEM (this work)	CMOS-only			M3D CMOS-NEM (this work)	CMOS-only		
		Pass gate	Transmission gate	Tri-state buffer		Pass gate	Transmission gate	Tri-state buffer
Max. freq. (GHz)	10.36	3.17	1.41	9.12	3.29	0.63	0.81	1.44
Power (μW)	3.42	5.26	10.52	188.78	82.81	323	175.03	752.42
Area (F^2)	480	1632	2784	3168	992	2528	4064	4576

✓ **Proposed M3D CMOS-NEM RL circuits exhibit 4.6x higher chip density, 2.3x higher operation frequency and 9.3x lower power consumption than CMOS-only ones in tile-to-tile operation, tri-state buffer case.**

Conclusion

- NEM memory based FPGAs are implemented. NEM memory based FPGAs can achieve low operation voltage, low energy consumption, high signal transfer speed compared with CMOS only FPGAs.
- Island style M3D CMOS-NEM RL circuits satisfying the V_{DD} requirement of the 65-nm CMOS technology node have been implemented and demonstrated for the first time.
- NEM memory routing switches are vertically integrated over CMOS logic circuits by using the CMOS baseline BEOL process. The only difference is HF vapor etching used to release the NEM structures.
- It is predicted that proposed M3D CMOS-NEM RL circuits will exhibit 4.6x higher chip density, 2.3x higher operation frequency and 9.3x lower power consumption than CMOS-only ones (tri-state buffer case) for tile-to-tile operation.