Multi-Layer Nanoelectromechanical (NEM) Memory Switches for Efficient Routing Operation

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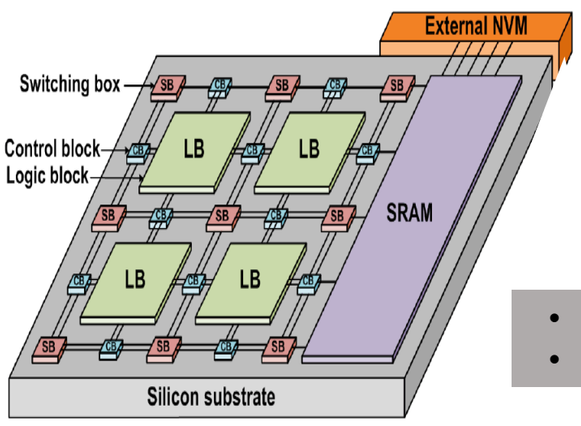
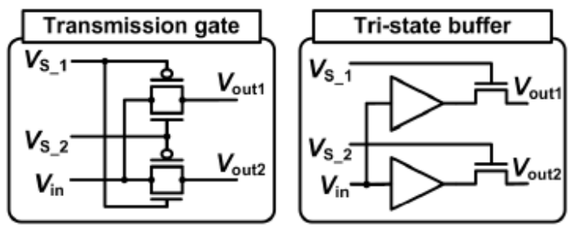
Motivation (1)

- **RL such as FPGA, CPLD consists of logic blocks and routing elements**
- **In conventional RL case, routing operation consumes ~ 80% of chip area, ~ 80% of core power and ~ 75% total delay**



✓ Routing elements

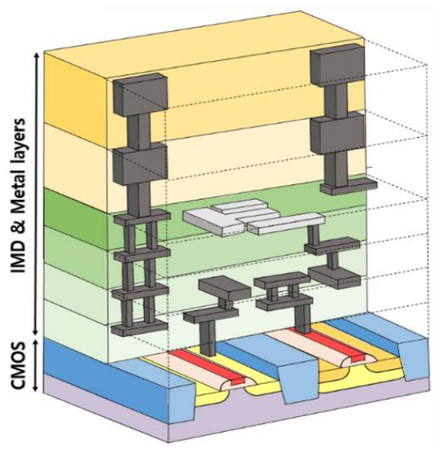


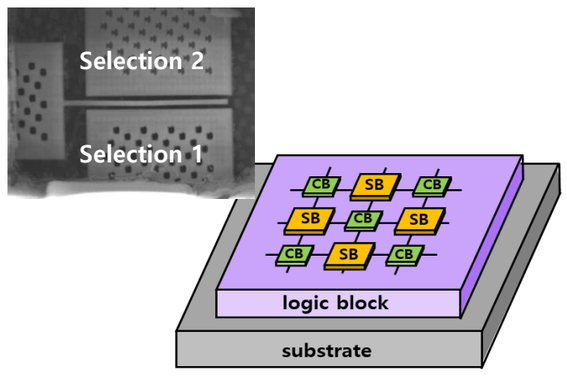
- **Low speed**
- **Low density**
- **Volatility**
- **High energy**

Need to decrease chip area, power consumption and delay

Motivation (2)

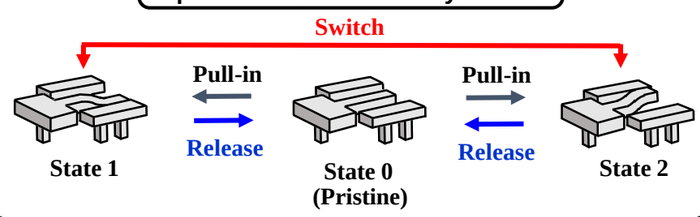
- **Replace routing elements from CMOS-only toNEM memory switch at single metal layer**
- **Routing elements located at BEOL**





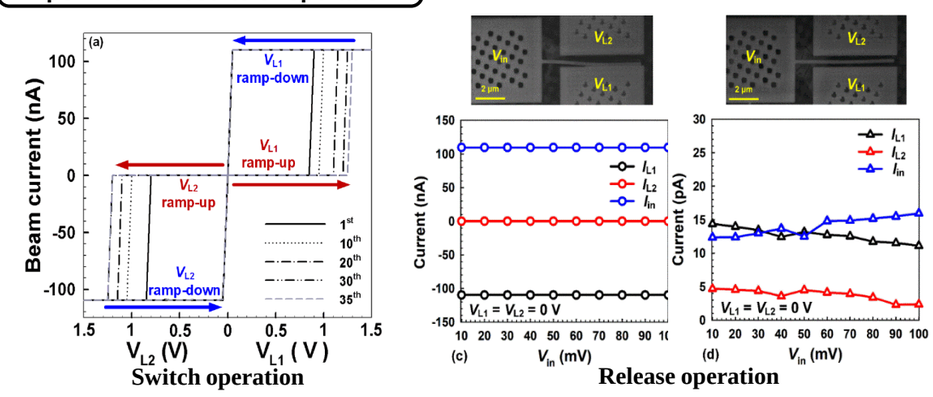
CMOS-NEM RL circuit

Operation of NEM memory switch



- **High speed**
- **High density**
- **Non-Volatility**
- **Low energy**

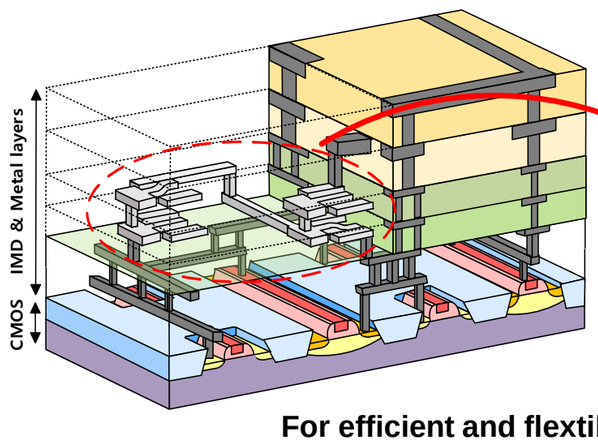
Experimental results of operation

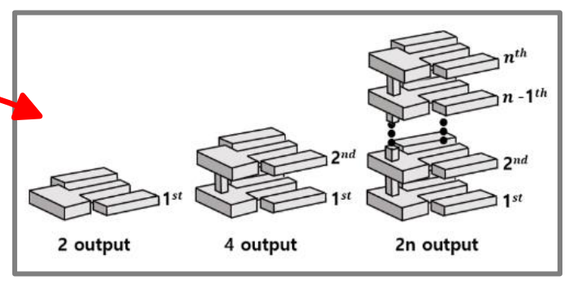


[H. S. Kwon *et al.*, *IEEE TED*, 2017]

[G. Baek *et al.*, *IEEE Access*, 2020]

Ideas

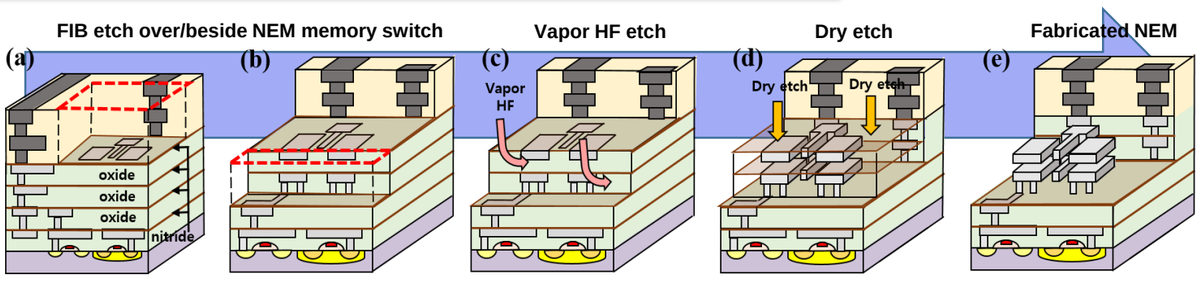




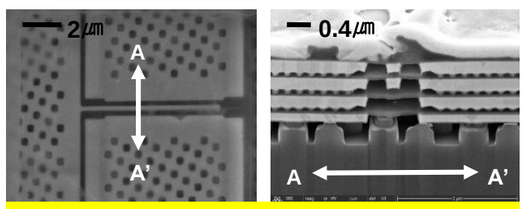
- Multi-layer NEM memory switch can be patterned at any metal lines

For efficient and flextible routing operation, multi-layer NEM memory switches are proposed

Fabrication process

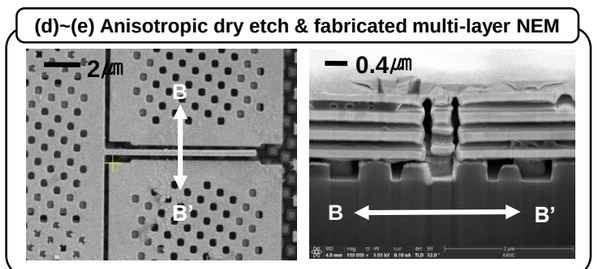


(c) Isotropic release by HF vapor



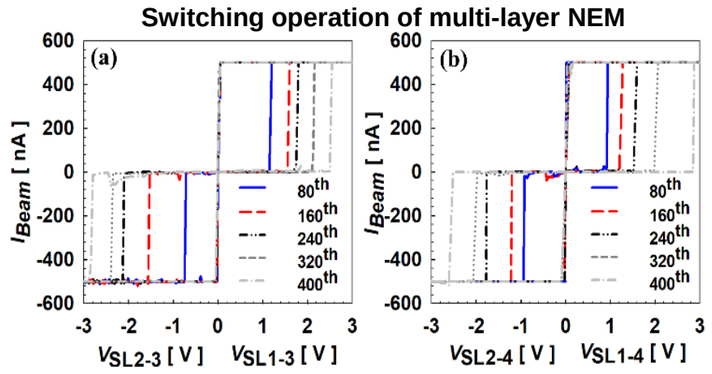
Nitride layers hold the beam when vapor HF is released

(d)~(e) Anisotropic dry etch & fabricated multi-layer NEM

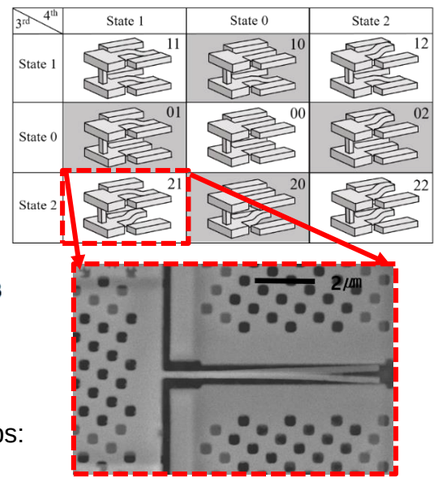


Experimental Results

Switching operation of multi-layer NEM

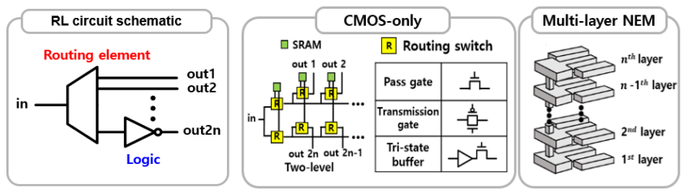


One of 3^2 feasible states

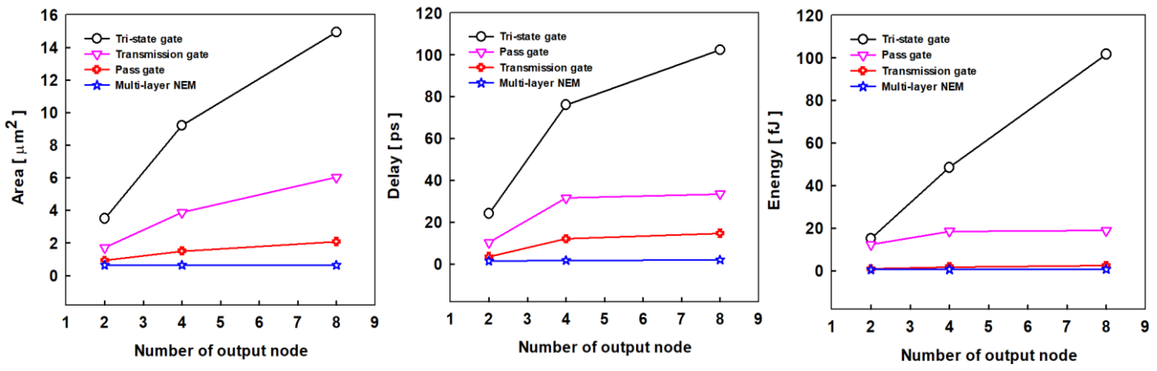


- The endurance cycle of the NEM memory switches exceeds 400 times within a 3-V range, which is comparable with the requirement of generic FPGA chips: ~500 times.

Simulation Results



✓ Multi-layer NEM memory switches enable more efficient data routing than conventional cases



Conclusion

- Multi-layer NEM memory switches integrated vertically over CMOS baseline circuits were experimentally demonstrated using a 65-nm CMOS baseline process
- By fabrication process, the throughput of NEM memory switch is increased than before process.
- The area, energy and power of multi-layer NEM memory switches are superior to CMOS-only routing elements
- An *n*-layer NEM memory switches can implement 3^n states which can be used for a 2*n*-to-1 multiplexer or 1-to-2*n* de-multiplexer

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